THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 47

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte SYUSO FUJII,
MITSURU SHIMIZU,
and KIYOFUMI SAKURAI

_____

Appeal No.1997-1696
Application 08/180,770[1]

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HEARD: DECEMBER 7, 1999

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Before FLEMING, RUGGIERO, and HECKER, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This a decision on appeal from the final rejection of claims 20 through 28, 30 through 34, 36

[1] Application for patent filed January 10, 1994. According to Appellants, this application is continuation of Application 07/793,421, filed December 13, 1991, now abandoned.

through 43 and 45, all of the claims pending in the present application.

Claims 1 through 19, 29, 35 and 44 have been canceled.

The invention relates to the method of testing input circuits, such as data-in buffer circuits or address buffers, for a semiconductor device. In particular, the method utilizes a test wherein a negative potential is applied to the semiconductor device. The method overcomes the prior art problem of generating minority carriers at a junction between the layer 22 and p-well region 26 as shown in figure 2 of the present application when a negative potential is applied V_{in} . On pages 8 and 9 of the specification, Appellants disclose that figure 4 shows a well region 16 is supplied with a potential which is lower and has a greater magnitude than the potential of input signal V_{in}. Appellants disclose that this arrangement prevents minority carriers generated when the potential V_{in} is negative. On pages 10 through 12 of the specification, Appellants disclose another embodiment shown in figure 6 in which a first power source potential V_{ss} is applied to the well regions 4 and 9 and a second power source potential V_{cc} is applied to a well region 14. Appellants disclose that the first power source potential V_{ss} is ground and the second power source potential V_{cc} is a potential greater than 0. Appellants disclose that under this arrangement the minority carriers generated at the junction portion between layers 4 and 6 when V_{in} is negative flow into well region 14. This overcomes the problem of the reduction to V_{ref} due to the injection of minority carriers.

Independent claims 20 and 25 are reproduced as follows:

20. A method of testing an input circuit, for a semiconductor device, that detects a level of an input signal V_{in} by comparing the input signal V_{in} with a reference signal V_{ref}, said input circuit comprising a semiconductor material of a first conductivity type, a first region of a second conductivity type opposite the first conductivity type in a surface portion of said semiconductor material, a second region of the first conductivity type in said first region, and a third region of the first conductivity type in said first region, said method comprising the steps of:

applying the input signal V_{in} to said second region, wherein V_{in} is negative;

applying the reference signal V_{ref} to said third region; and

applying to said first region a potential which is lower and has a greater magnitude than the potential of the input signal V_{in} thereby preventing an injection of carriers generated at a junction between said first and second regions into said third region.

25. A method of testing an input circuit, for a semiconductor device, that detects a level of an input signal V_{in} by comparing the input signal V_{in} with a reference signal V_{ref}, said input circuit comprising a semiconductor material of a first conductivity type, first and second spaced regions of a second conductivity type opposite the first conductivity type in a surface portion of said semiconductor material, a first input field effect transistor formed in said first region and including a first current terminal region of the first conductivity type, a second input field effect transistor formed in said second region and including a first current terminal region of the first conductivity type, a third region of the first conductivity type between said first and second spaced regions, said method comprising the steps of:

applying a first power source potential to said first region;

applying the first power source potential to said second region;

applying the reference signal V_{ref} to the first current terminal of said first input field effect transistor;

applying the input signal V_{in} to the first current terminal of said second input field effect transistor, wherein V_{in} is negative; and

applying to said third region a second power source potential higher than the first power source potential thereby preventing an injection of carriers generated at a junction between said first region and the first current terminal region of said first input field effect transistor into the first current terminal region of said second input field effect transistor.

The Examiner relies on the following references:

Suzuki et al. (Suzuki) 4,233,672 Nov. 11, 1980

Admitted prior art Figures 1 and 2

Claims 20 through 28, 30 through 34, 36 through 43 and 45 stand rejected under 35 U.S.C. § 103 as being unpatentable over Suzuki in view of Appellants' prior art figures 1 and 2.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief[2] and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 20 through 28, 30 through 34, 36 through 43 and 45 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or

[2] Appellants filed an appeal brief on August 7, 1996. Appellants filed a reply brief on December 17, 1996. The Examiner mailed a communication on February 13, 1997 denying entry of the reply brief. Therefore, the reply brief is not properly before us for our consideration.

suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). We note that our reviewing court states that "when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On pages 8 through 11 and 15 of the brief, Appellants argue in regard to claims 20 through 24, 31, 32 and 36 through 39 that neither Suzuki nor the admitted prior art figures 1 and 2 teaches or suggests that the specific potential applied to the first region has a potential which is lower and has a greater magnitude than the potential of the input signal V_{in}. In regard to claims 25 through 28, 30, 33, 34, 40 through 43 and 45, Appellants argue on pages 12 through 15 of the brief that neither Suzuki nor the prior art figures 1 and 2 teaches or suggests applying a first power source potential to the first region and to the second region, applying the reference signal V_{ref} to the first current terminal of the first input field effect transistor, applying the input signal V_{in} to the first current terminal of the second input field effect transistor, and applying to the third region a power source potential higher than the first power source potential under a test condition.

We note that Appellants' claim 20 recites "applying to said first region a potential which is lower and has a greater magnitude than the potential of the input signal V_{in} thereby preventing an injection of carriers generated at a junction between said first and second regions into said third region." Furthermore, we note that independent claims 22, 23, 31, 32, 36 and 38 recite similar language.

We agree with the Examiner that Suzuki teaches the same structure as recited in the preamble of Appellants' claim 20. However, we fail to find that Suzuki teaches the method of testing and, in particular, applying to said first region a potential which is lower and has a greater magnitude than the potential of the input signal V_{in} thereby preventing an injection of carriers generated at a junction between said first and second regions into said third region. Furthermore, we note that Appellants' prior art figures 1 and 2 do not provide the above limitation as well. The Examiner has not provided any evidence of such teachings in the prior art.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Piasecki,*** 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984); ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966).

Furthermore, our reviewing court states in ***In re Piasecki***, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984) the following:

> The Supreme Court in ***Graham v. John Deere Co.***, 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under section 102 and 103". ***Citing In re Warner***, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967).

We note that Appellants' claim 25 recites "applying to said third region a second power source potential higher than the first power source potential thereby preventing an injection of carriers generated at a junction between said first region and the first current terminal region of said first input field effect transistor into the first current terminal region of said second input field effect transistor." We note that independent claims 33 and 40 recite similar limitations.

We question whether the Examiner has shown that Suzuki teaches the structure set forth in the preamble of independent claim 25. However, even if the Examiner has shown such structure, we fail to find that Suzuki teaches the method of testing as recited in independent claims 25, 33 and 40. In particular, we fail to find that Suzuki or the admitted prior art figures 1 and 2 teaches the above limitation of applying to the third region a second power source potential higher than the first power source potential thereby preventing an injection of carriers. Again, the Examiner has not provided any evidence that these methods steps are known in the prior art.

In view of the foregoing, we have not sustained the rejection of claims 20 through 28, 30 through 34, 36 through 43 and 45 under 35 U.S.C. § 103.

Accordingly, the Examiner's decision is reversed.

REVERSED

MICHAEL R. FLEMING	)
Administrative Patent Judge	)
	)
	)
	) BOARD OF PATENT
JOSEPH F. RUGGIERO	)
Administrative Patent Judge	) APPEALS AND
	)
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STUART N. HECKER	)
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